



Fr. Conceicao Rodrigues College of Engineering

Father Agnel Ashram, Bandstand, Bandra –west, Mumbai-50

Department of Computer Engineering

Practical Plan

Class: SE Comps DIV-B		Weekly Schedule:				
Course name/code: Digital Logic & Computer Organization		Batch A: Tuesday 1:30m pm to 3:30 pm				
Academic Year: 2023-24		Batch B: Monday 1:30m pm to 3:30 pm				
Name of the teacher: Prof. Heenakausr pendhari/		Batch C: Friday 11am to 1 pm				
		Batch D: Wednesday 1:30m pm to 3:30 pm				
Course Outcomes:						
CSL302.1 Design and simulate digital components and circuits to perform arithmetic and logical operations.						
CSL302.2 Demonstrate the working of ALU and CPU in computers.						
CSL302.3 Implement various algorithms for arithmetic operations in a programming language.						
CSL302.4 Construct cache memory using different mapping techniques and software tools.						
Sr. No.	Title of experiment	Course Outcomes	Batch	Planned date	Actual date	Remark
1	Verification of Truth table of various logic gates	CSL302.1	A	25/7/2023		
			B	24/7/2023		
			C	28/7/2023		
			D	26/7/2023		
2	Realization of Half Adder and Full Adder using logic gates	CSL302.1	A	1/8/2023		
			B	31/7/2023		



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			C	4/8/2023	
			D	2/8/2023	
3	Design and realization of logic function using Multiplexer(IC74151) / Decoder (74138)	. CSL302.1	A	8/8/2023	
			B	7/8/2023	
			C	11/8/2023	
			D	9/8/2023	
4	Verification of working of various Flipflops	CSL302.1.	A	22/8/2023	
			B	14/8/2023	
			C	18/8/2023	
			D	23/8/2023	
5	Ripple Carry Adder	CSL302.1	A	5/9/2023	
			B	21/10/2023	
			C	25/8/2023	
			D	6/9/2023	
6	Design and implement 4-bit and 16-bit ALU	CSL302.2	A	12/9/2023	
			B	4/9/2023	
			C	1/9/2023	
			D	13/9/2023	
7	Design and implement Control Unit	CSL302.2	A	26/19/2023	
			B	11/9/2023	
			C	8/9/2023	
			D	27/9/2023	
8	Write a program for binary multiplication.(Booth's Algorithm)	CSL302.3	A	3/10/2023	
			B	18/9/2023	
			C	15/9/2023	



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			D	4/10/2023	
9	Write a program to implement Restoring/Non Restoring algorithm for Division.	CSL302.3	A	17/10/2023	
			B	25/09/2023	
			C	27/09/2023	
			D	18/10/2023	
10	Cache Mapping	CSL302.4	A	21/10/2023(extra)	
			B	16/10/2023	
			C	6/10/2023	
			D	21/10/2023(extra)	
11	Demonstration of Shift register using 94194	CSL302.1	A	23/10/2023	
			B	23/10/2023	
			C	23/10/2023	
			D	23/10/2023	Extra for All four batches